High-Level Hardware-Software Codesign of an 802.11a Transceiver System using Zynq SoC

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Abstract

- Modern wireless protocols are constantly evolving to suit more devices.
- Heterogeneous computing lets behaviors map to different processing elements (HW/SW).
- Prototype 802.11a transceiver using Xilinx Zynq Z-7000 SoC & AD-FMCMMS3-EZB RF board.
- Use MathWorks SW tools for building HDL and C code to interface with the radio.
- Results: measure max PS step time & FPGA utilization to select codesign configuration.

Hardware Setup

- AXI interconnect (bus) manages data streams.
- Features AD9361 wideband scrambler: XOR to make data pseudorandom, unbiased, independent.
- Convolutional Encoding: adds redundancy, produces parity bits with Boolean polynomial function.
- Orthogonal Frequency Division Multiplexing (OFDM): IFFT to carry data on multiple channels.

Results

- Maximum PS step time decreases as more components moved to PL.
- Moving IFFT (OFDM Modulation) to PS reduces max step time.
- Further optimizations needed to reduce to standard 4 μs step time.
- Increase in resource utilization (LUT & register usage) as V# increases.
- In all model variants, FPGA at <5% utilization; meaning there’s still room for Rx & higher OSI layers.

Design Challenges

- What is the best way to partition transceiver subsystem blocks between the Zynq PL & PS?
- Reconfiguring Simulink models to effect proper HDL generation to build an accurate and time-efficient PL image that can be turned into a bitstream file for the Zynq SD card.
- Similar model to generate and build time-efficient C code targeted for the PS ARM.

Future Work

- Perform tests with live, online radio transmissions.
- Measure packet error rate (PER) for different codesigns.
- Use study as basis for multiple-input, multiple-output (MIMO) and higher layers (e.g. MAC).
- Apply same system design principles to more modern wireless standards.
- e.g. 802.11ac for beamforming, 802.11af for UHF band reuse, 4G LTE.

References


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